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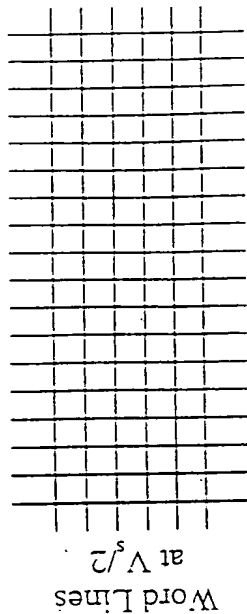


FIG. 2

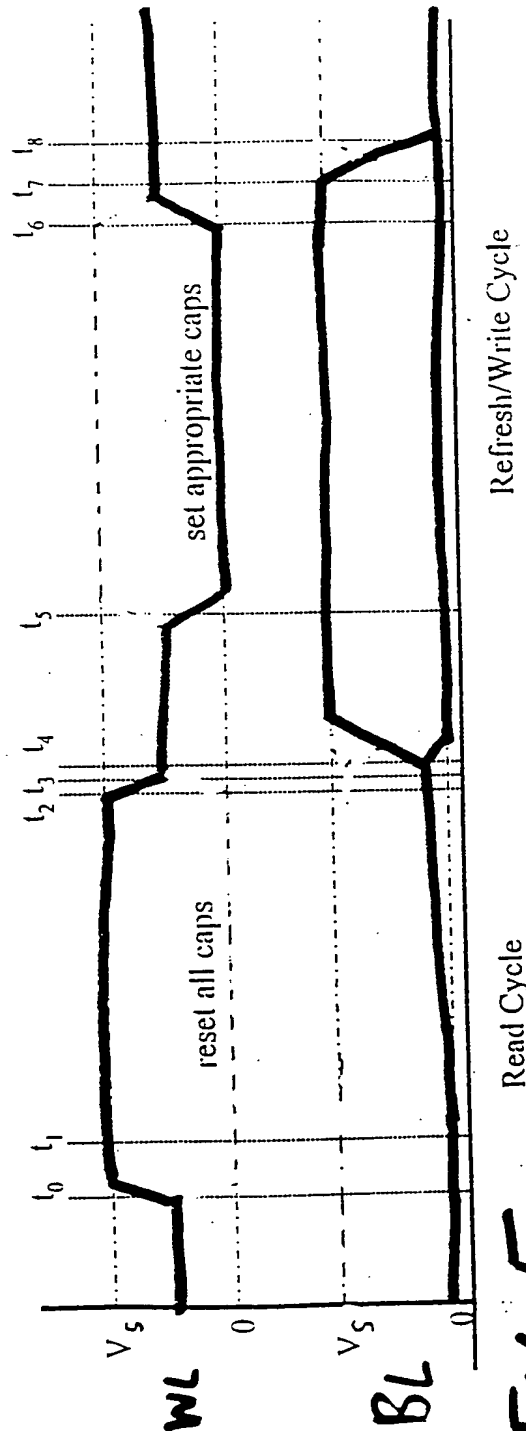
3 Level Passive Matrix Switching Protocol

Maximum depolarizing voltage $V_s/2$

- t_0 : word line latched, active pull μp to V_s
- t_1 : bit line clamp released - sense amp on
- t_2 : bit line decision - data latched
- t_3 : word line returned to quiescent $V_s/2$
- t_4 : write data latched on bit lines
- t_5 : word line pulled to 0 - set/reset caps
- t_6 : word line returned to quiescent $V_s/2$
- t_7 : bit lines actively returned to 0 clamp
- t_8 : read/write cycle complete



Sense Amps biased near V_s



Refresh/Write Cycle

Read Cycle

FIG. 5

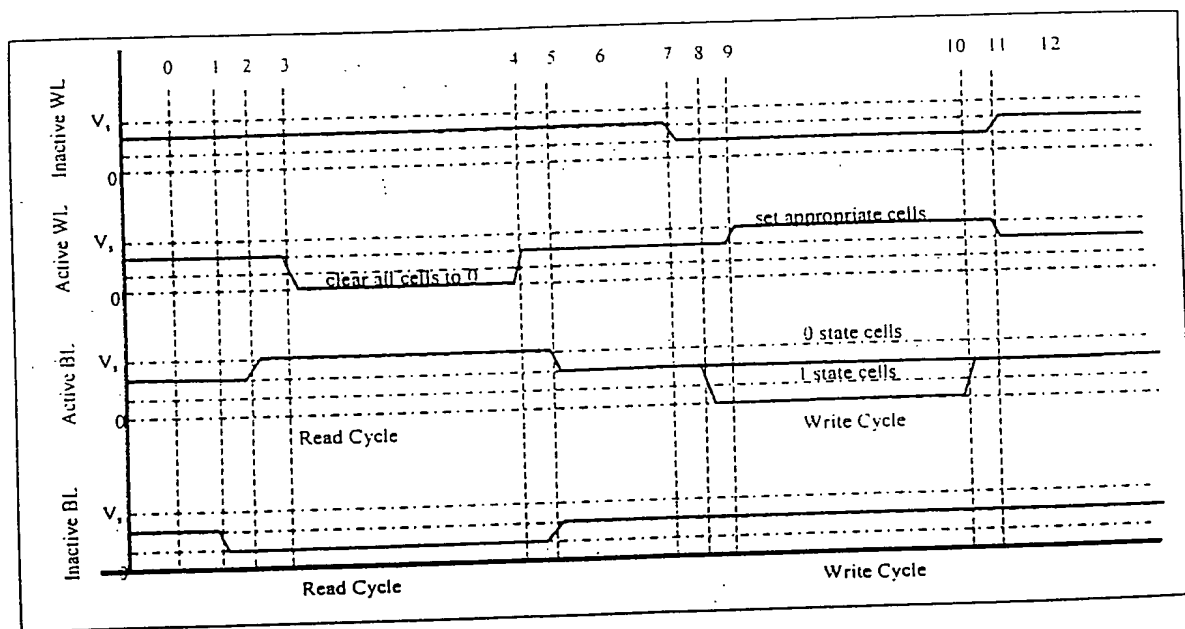


FIG. 6.

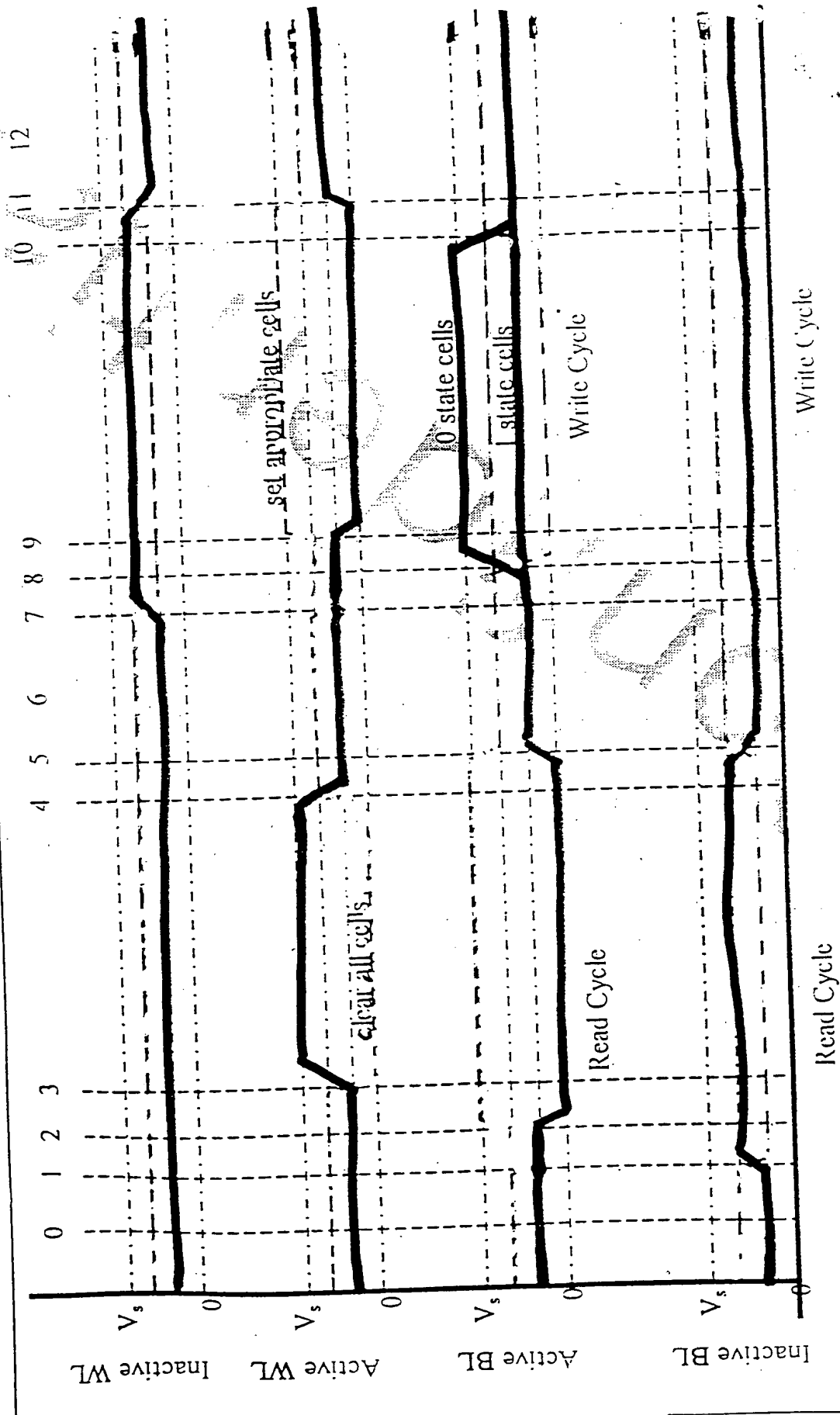


FIG. 7

Five Level Timing Diagram

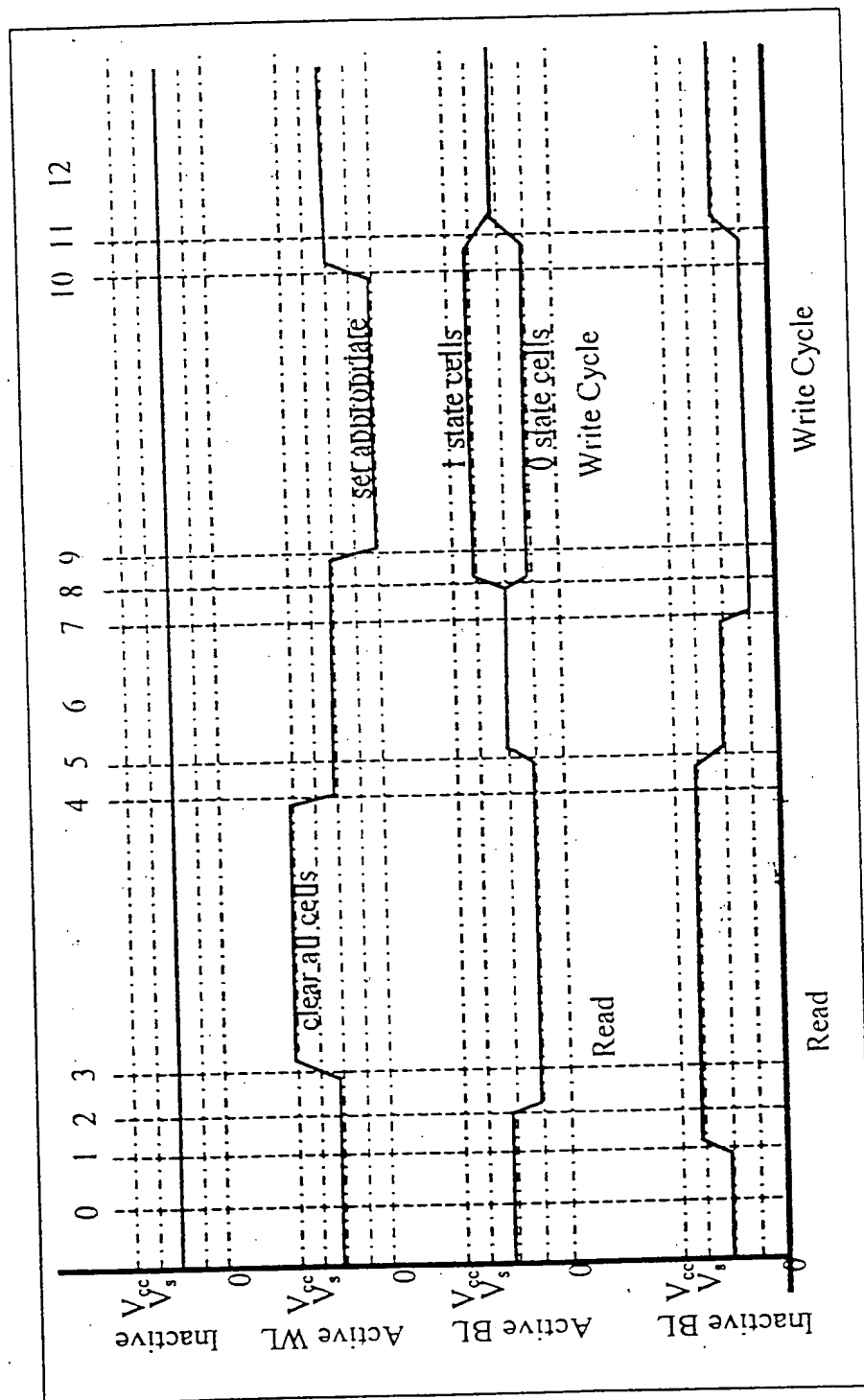


FIG. 9

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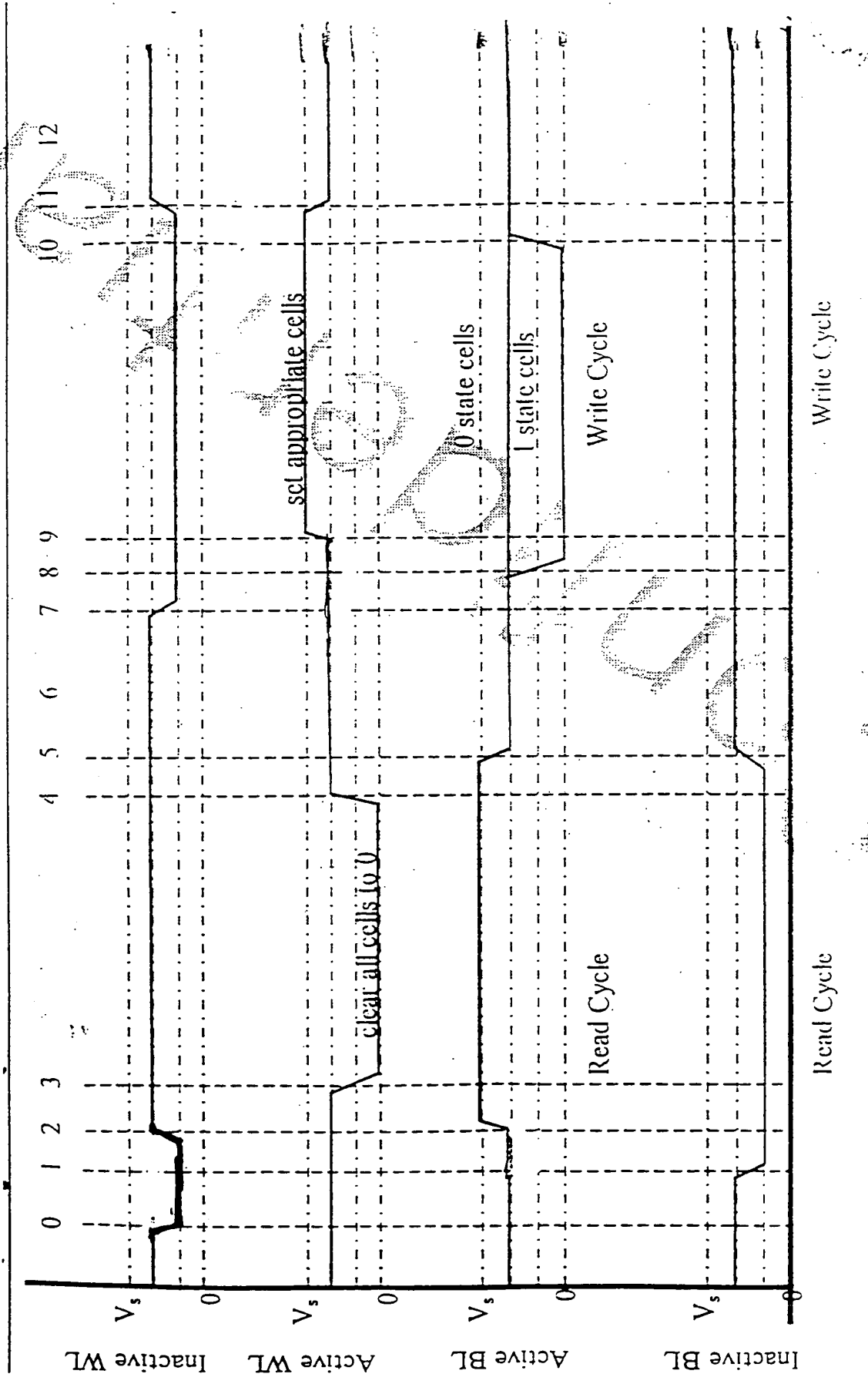


Fig. 10

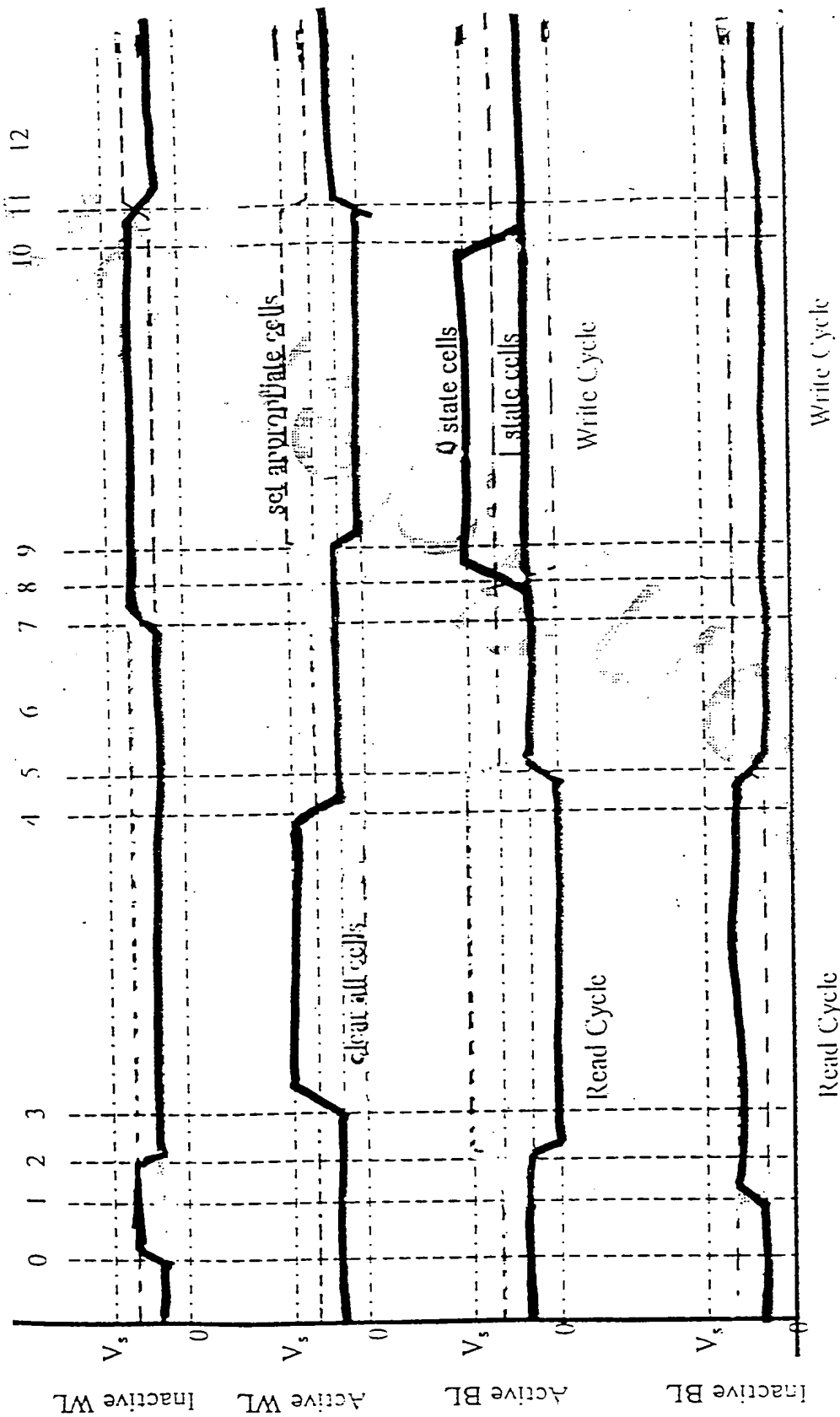


Fig. 11

The timing diagram illustrates the sequence of operations for the 74VHC000. It shows the relationship between the clock signal (WL) and the data bus (BL) during a Read Cycle and a Write Cycle. The clock cycles are numbered 0 to 12. The diagram includes signals for V_{cc} , V_{ss} , Inactive WL, Active WL, Active BL, and Inactive BL. Key events are annotated: 'clear all cells to 0' occurs during the first Read Cycle; 'set appropriate cells' occurs during the first Write Cycle; '0 state cells' and '1 state cells' are indicated during the second Read Cycle. The Read Cycle is labeled 'Read Cycle' and the Write Cycle is labeled 'Write Cycle'.

FIG. 12

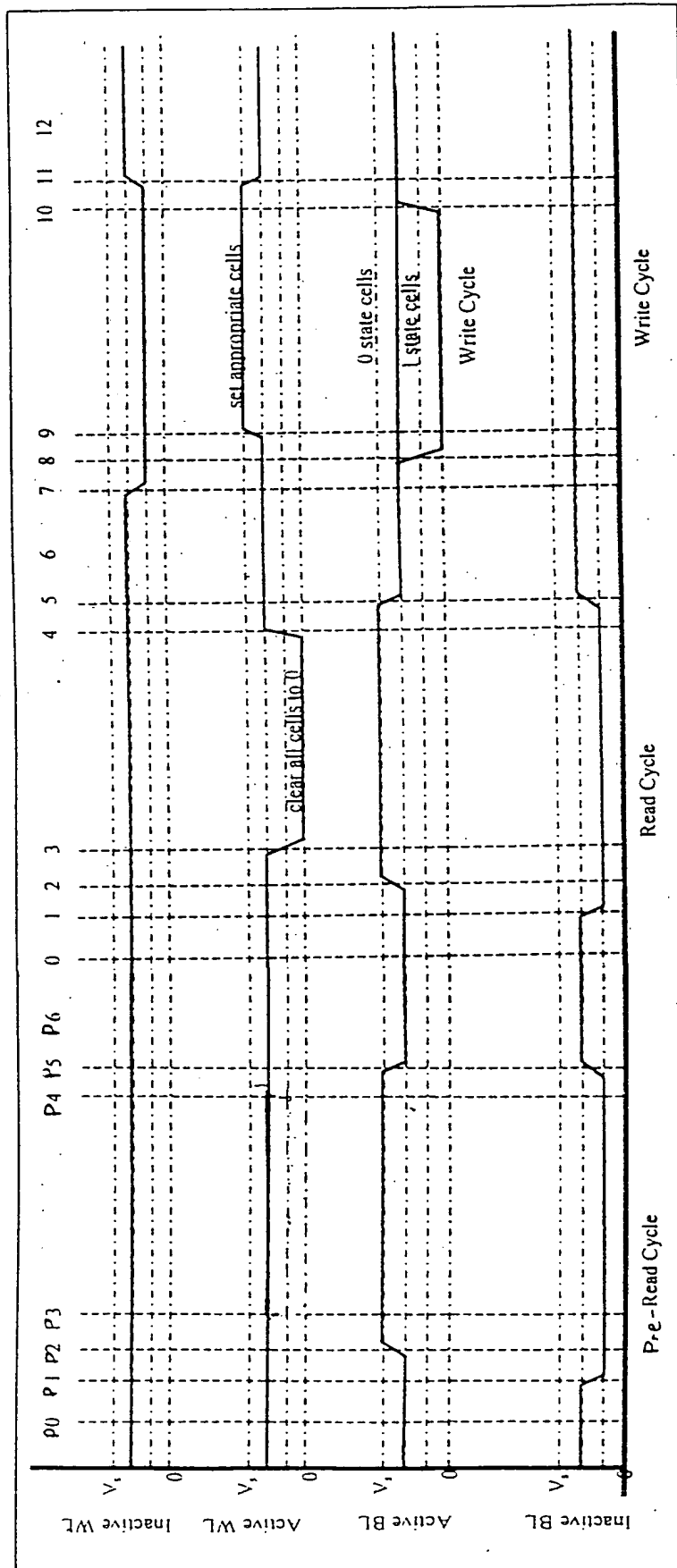


FIG. 14
EXAMPLE OF READ AND WRITE PROTOCOL INVOLVING A PRE-READ REFERENCE CYCLE.

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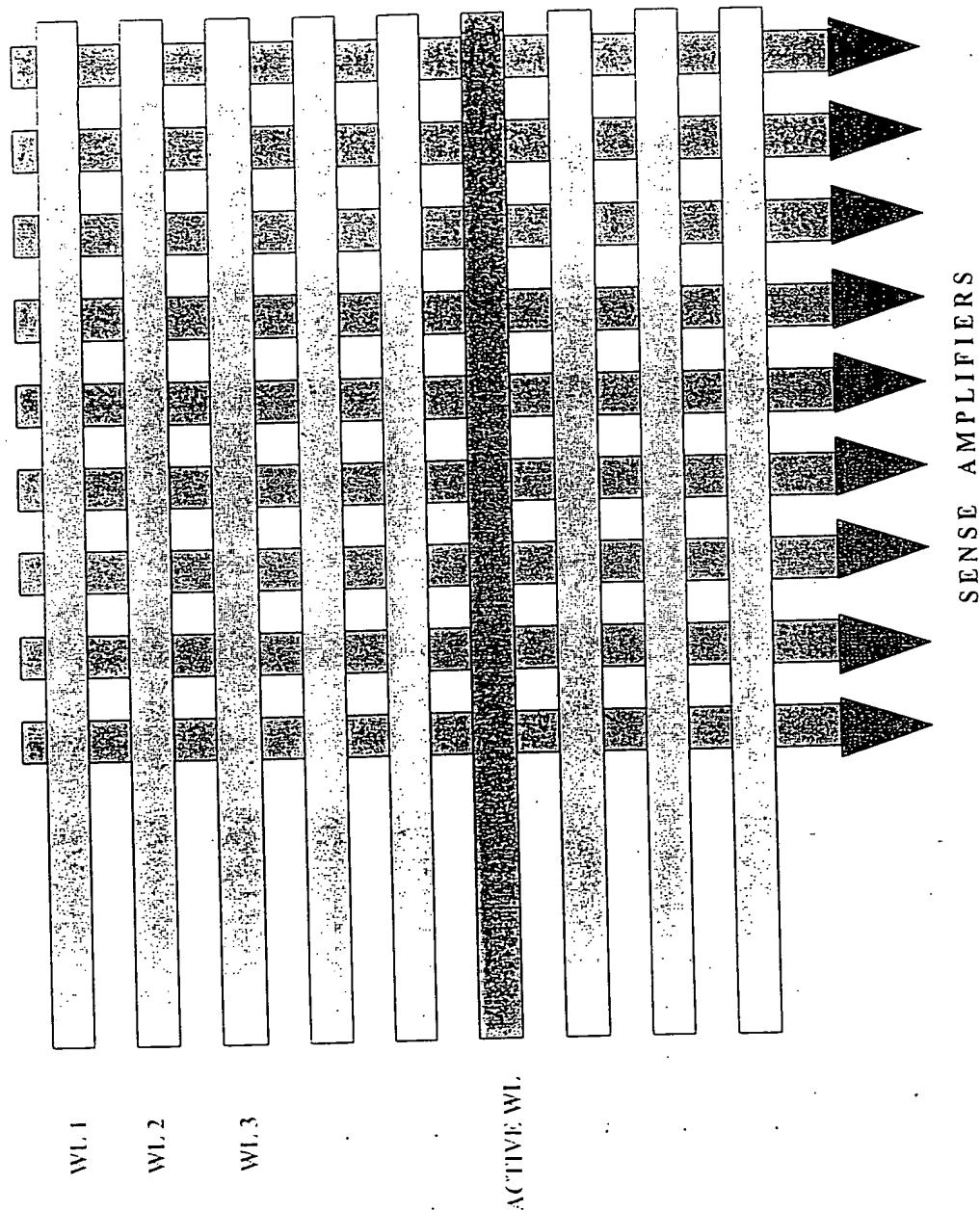


FIG.15

BL 1 BL 2 BL 3